FAIRCHILD SEMICONDUCTOR™

February 2001
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FSLV16211
24-Bit Bus Switch

General Description

The FSLV16211 is a 24-bit, high speed, low voltage bus switch. The low On Resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

This device's design allow this part to be used as a 12-bit or 24-bit bus switch. When $\overline{OE}_1$ is LOW, Port 1A is connected to Port 1B. When $\overline{OE}_2$ is LOW, Port 2A is connected to Port 2B.

Features

- 5Ω switch connection between two ports
- Minimal propagation delay through the switch
- Low I_{CC}
- Zero bounce in flow-through mode
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

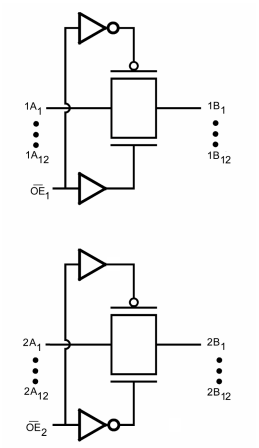
Ordering Code:

Order Number	Package Number	Package Description
FSLV16211GX (Note 1)	BGA54A	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide (TAPE and REEL)
FSLV16211MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

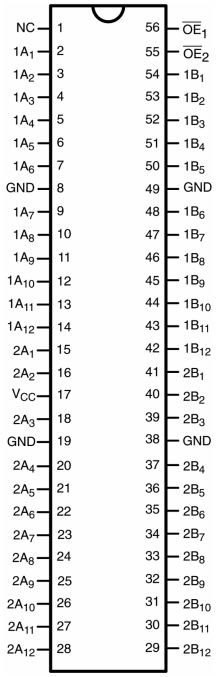
Note 1: BGA package available in Tape and Reel only.

Logic Diagram

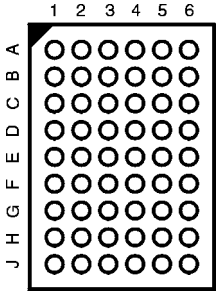


Connection Diagrams

Pin Assignment for TSSOP



Pin Assignment for FBGA



(Top Thru View)

Pin Descriptions

Pin Name	Description
$\overline{OE}_1$, $\overline{OE}_2$	Bus Switch Enables
1A, 2A	Bus A
1B, 2B	Bus B
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
A	$1A_2$	$1A_1$	NC	OE_2	$1B_1$	$1B_2$
B	$1A_4$	$1A_3$	$1A_7$	OE_1	$1B_3$	$1B_4$
C	$1A_6$	$1A_5$	GND	$1B_7$	$1B_5$	$1B_6$
D	$1A_{10}$	$1A_9$	$1A_8$	$1B_8$	$1B_9$	$1B_{10}$
E	$1A_{12}$	$1A_{11}$	$2A_1$	$2B_1$	$1B_{11}$	$1B_{12}$
F	$2A_4$	$2A_3$	$2A_2$	$2B_2$	$2B_3$	$2B_4$
G	$2A_6$	$2A_5$	V_{CC}	GND	$2B_5$	$2B_6$
H	$2A_8$	$2A_7$	$2A_9$	$2B_9$	$2B_7$	$2B_8$
J	$2A_{12}$	$2A_{11}$	$2A_{10}$	$2B_{10}$	$2B_{11}$	$2B_{12}$

Truth Table

Inputs		Inputs/Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

Absolute Maximum Ratings(Note 2)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Switch Voltage (V_S)	−0.5V to +4.6V
DC Input Voltage (V_{IN}) (Note 3)	−0.5V to +4.6V
DC Input Diode Current (I_{IK}) V_{IN} < 0V	−50 mA
DC Output (I_{OUT}) Sink Current	128 mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/− 100 mA
Storage Temperature Range (T_{STG})	−65°C to +150 °C

Recommended Operating Conditions (Note 4)

Power Supply Operating (V_{CC})	2.3V to 3.6V
Input Voltage (V_{IN})	0V to 3.6V
Output Voltage (V_{OUT})	0V to 3.6V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0 ns/V to 4 ns/V
Switch I/O	0 ns/V to DC
Free Air Operating Temperature (T_A)	-40 °C to +85 °C

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 4: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics (Note: Not all conditions may appear on all switch types)

Symbol	Parameter	V_{CC}	T_A = −40 °C to +85 °C			Units	Conditions
		(V)	Min	Typ	Max		
V_{IK}	Clamp Diode Voltage	3.0			−1.2	V	I_{IN} = −18 mA
V_{IH}	HIGH Level Control Input Voltage	2.3-2.7	1.7			V	
		2.7-3.6	2.0				
V_{IL}	LOW Level Control Input Voltage	2.3-2.7			0.7	V	
		2.7-3.6			0.8		
I_I	Input Leakage Current	2.3			10	μA	Force V_I = 3.6V, I_{OUT} = 0.0A
		0.0			10		Force V_I = 3.6V
		3.6			1		0 ≤ V_{IN} ≤ 3.6V
I_{CC}	Quiescent Supply Current	3.6			3	μA	V_{IN} = V_{CC} or GND, I_{OUT} = 0A
ΔI_{CC}	Increase in I_{CC} per Input	3.6			300	μA	One Input @ 3V, Other Inputs at V_{CC} or GND
I_{OZ}	OFF-STATE Leakage	3.6			±1	μA	0.0 ≤ A, B ≤ 3.6V
R_{ON}	Switch On Resistance	3.0		5	7	Ω	I_{IN} = 64 mA, V_I = 0.0V
		3.0		5	7		I_{IN} = 30 mA, V_I = 0.0V
		3.0		10	15		I_{IN} = 15 mA, V_I = 2.4V
		3.0			20		I_{IN} = 15 mA, V_I = 3.0V
		2.3		5	8		I_{IN} = 64 mA, V_I = 0.0V
		2.3		5	8		I_{IN} = 30 mA, V_I = 0.0V
		2.3		10	15		I_{IN} = 15 mA, V_I = 1.7V
		2.3			20		I_{IN} = 15 mA, V_I = 2.0V

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 30pF$, $R_L = 500\Omega$		$T_A = -40°C$ to $+85°C$, $C_L = 50pF$, $R_L = 500\Omega$		Units
		$V_{CC} = 2.5V \pm 0.20V$		$V_{CC} = 3.3V \pm 0.30V$		
		Min	Max	Min	Max	
t_{PHL}, t_{PLH}	Propagation Delay (Note 5)		0.15		0.25	ns
t_{PHZ}, t_{PLZ}	Enable Time	0.5	4.7	1.0	7.0	ns
t_{PZH}, t_{PZL}	Disable Time	0.5	5.1	1.0	5.5	ns

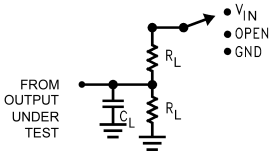
Note 5: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On Resistance of the switch and the load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 6)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Pin Input Capacitance	4.5		pF	$V_{CC} = 3.3V$
$C_{I/O}$	Input/Output Capacitance	6.5		pF	V_{CC}, $\overline{OE} = 3.3V$

Note 6: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Test	Switch
t_{PD}	Open
t_{PLZ}/t_{PZL}	V_{IN}
t_{PHZ}/t_{PZH}	GND

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, $t_W = 500$ ns

FIGURE 1. AC Test Circuit

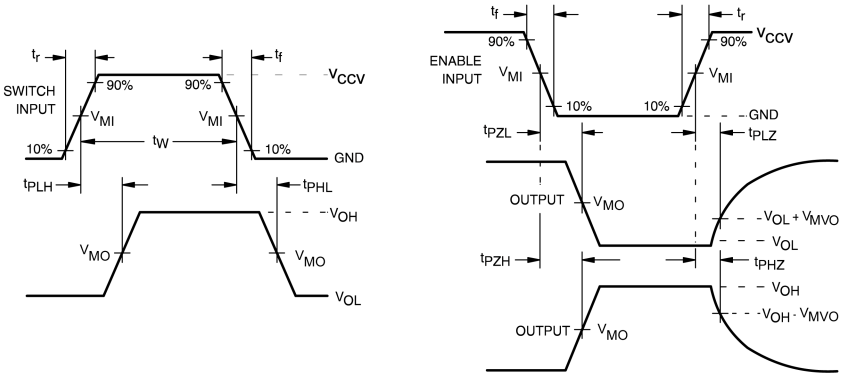
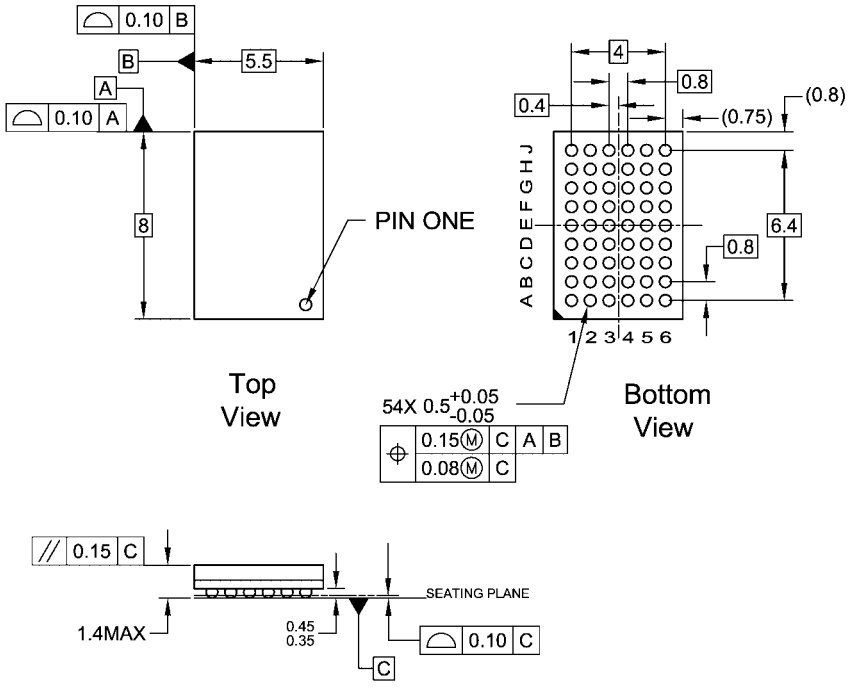


FIGURE 2. AC Waveforms

	V_{CC}	
Symbol	**$3.3V \pm 0.3V$**	**$2.5V \pm 0.2V$**
V_{MI}	1.5V	$V_{CC}/2$
V_{MO}	1.5V	$V_{CC}/2$
V_{MVO}	0.3V	0.15V
V_{IN}	6.0V	$2 \times V_{CC}$
V_{CCV}	3.0	V_{CC}
t_r/t_f	2 ns	2.5 ns

Physical Dimensions inches (millimeters) unless otherwise noted



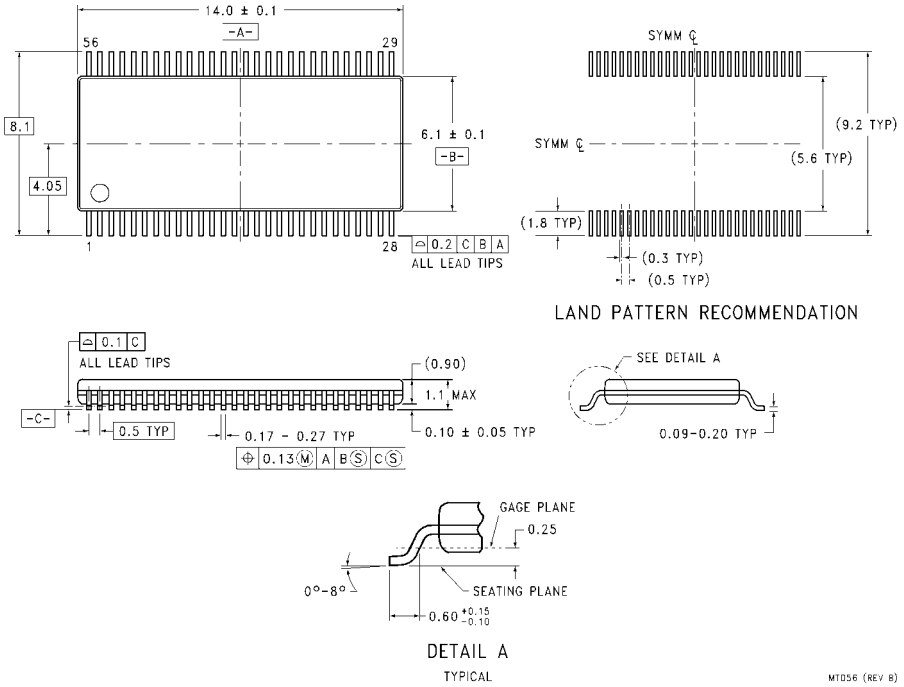
NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.